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MODERN IMPLEMENTATION OF JOHNSON COUNTER IN LOW POWER DIGITAL LOGICS USING CLOCK TIMING TECHNIQUES

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ABSTRACT

The instinctive purpose of this study is to make VLSI circuits as low power consuming as possible. A lot of work has been done to reduce the operational power dissipation of the circuit, and reducing the power of sequential circuits is most important as it has clock as one of its input. Johnson counters are the sequential circuits which have so many unwanted switching of the clock pulses. Clock gating is the technique which reduces the power dissipation by eliminating the unwanted switching of the clock pulses. In this technique, the clock is supplied when output is different from the input and the clock is suppressed when output is same as the input. A new design of Johnson counter was studied in which additional circuitry of clock gating was used the unnecessary switching of the clock pulses and thus, to improve the power dissipation. It reduced the power to appreciable amount but this logic increased the chip area increasing the number of transistors. In this design, the optimization can be done in various blocks. Flip-flop being used in master slave mode consume huge power and the logic gates are also the site of power dissipation. So, a new design is proposed which comprises of proposed flip-flop design and modified logic gates design and a proposed design is simulated with the help of HSPICE which gives huge power reduction.

KEYWORDS: Johnson Counter, Flip Flop, Clock, HSPICE.

1. INTRODUCTION

In recent years, the demand for power-efficient designs has grown significantly. This tremendous demand has mainly been due to the continuous growth of battery-operated portable applications. Power dissipation minimization has become the main design issue in the VLSI circuits with the shrinking of chip sizes & higher operational frequencies of the devices. Due to higher operational frequency, chip power dissipation increases which requires more expensive packaging & cooling strategies and also degrades system reliability. With the growing demand of the portable electronic devices like smartphones, laptops, notebook computers, PDAs etc. which require higher performance with greater functionality, minimizing power dissipation has become an important factor in such system.

As the technology progresses, the number of transistors integrated on a single chip increases which causes increase in the chip power. Supply voltage is scaled to maintain the power consumption within limit but scaling of supply voltage is limited by the high-performance requirement. Hence, the scaling of supply voltage only may not be sufficient to maintain the power density within limit, which is required for the power-sensitive applications. Circuit technique and system-level techniques are also required along with supply voltage scaling to achieve low-power designs. The operations in sequential circuits are executed on the clock transition edge (either on positive or on negative clock edge) but at every clock transition there will always be a short circuit current dissipation which contributes almost 15-45% of the power dissipation in the system. Low power design of sequential circuits can be ensured by using clock gating technique where unnecessary clock transitions are eliminated & clock pulse sequences are provided to the flip flops only when an operation needs to be performed. As clock signals do not perform any computation and is mainly used for the synchronization. Hence, these signals do not contain any

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information. So by using clock gating, power dissipation can be minimized by reducing unnecessary clock activities.

High performance systems dissipate more chip power which requires increasingly expensive packaging & cooling strategies and also degrades system reliability. Consequently, there is a financial advantage to reducing the power consumed in high performance systems. Another crucial driving factor is that excessive power consumption is becoming the limiting factor in integrating more transistors on a single chip or on a multiple-chip module. Unless power consumption is dramatically reduced, the resulting heat will limit the feasible packing and performance of VLSI circuits and systems.

Designing a low power circuit involves a proper architecture of the sequential and combinational circuits used in the design by using minimum CMOS logic gates and then eliminating the redundant operations by using efficient techniques. Sequential circuits such as counters and registers are omnipresent in the modern day designs. In a typical design, all computer operations (arithmetic, logical, and memory processes) are executed synchronously with respect to the clock transition edges (either on positive or on negative clock edge) but at every clock transition there will always be a short circuit current dissipation which contributes almost 15-45% of the power dissipation in the system. The low power design of sequential circuits can be ensured by using clock gating technique where unnecessary clock transitions are eliminated & clock pulse sequences are provided to the flip flops only when an operation needs to be performed.

As flip flops are the fundamental building blocks of any sequential circuit so the performance of flip flops has a larger impact on the circuit speed and power consumption. For implementing efficient design of any digital circuit, it is necessary to minimize dissipated power in both clock distribution networks and flip-flops. In order to improve the performance of flip flop architecture and to reduce the power consumption extensive work has been carried out in the past few decades.

Counters are the sequential circuits consisting of set of flip flops connected in a suitable manner to count the sequence of the input pulses in a specified time period. Johnson Counter provides special kinds of data sequences synchronously, which are essential in various important applications (e.g. D/A converter, FSMs, and clock dividers).In this dissertation, a 4-bit low power design of Johnson counter has been proposed which uses pulse-triggered flip flop instead of conventional Master-Slave flip flop & GDI based clock gated logic function. The proposed design shows a significant reduction in power dissipation as compared to the existing clock gated Johnson counter design.

2. MATERIALS AND METHODS

Low power digital cmos design

2.1 Power dissipation in digital CMOS circuits

Power dissipation in CMOS digital circuits is categorized into two types: Peak power & Average power. Peak power affects both circuit lifetime and performance. Excessive instantaneous current drawn from the power supply results in a voltage drop over the supply rails and causes a large power dissipation which causes overheating of the device that reduces the system reliability and lifetime of the circuit. Also, voltage drop along the supply lines hinders the performance of the circuit & causes erroneous digital outputs.

Average power dissipation is significant for calculating the battery weight & lifetime. Average power is categorized into: Dynamic power and Static power dissipation. Dynamic power is the component proportional to the operating frequency of the device or the frequency of the node switching. Dynamic power is important during normal operation especially at high operating frequencies whereas static power is more important during standby especially for battery powered devices.

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2.2 Dynamic Power Dissipation

Dynamic power consists of two components: Switching power that occurs due to charging and discharging of Load capacitance & Short circuit power which is due to non-zero rise time & fall time of input waveforms.

2.2.1 Switching Power Dissipation

Switching power is defined as the power consumed by the logic gate to charge the output load from the low voltage level '0' to the high voltage level '1'. Fig.1 shows the charging and discharging of load capacitance in a CMOS inverter. Initially, when input (V_{IN}) is 0, then NMOS is OFF & PMOS is conducting which charges the load capacitor up to V_{DD} through PMOS transistor i.e. energy is transferred from the voltage source to the load capacitor but only half of this energy is stored on the capacitor ($E_C = ½ C_{LOAD} V_{DD}^2$) & other half is dissipated in PMOS as heat. When input switches from 0 to 1 then the charge stored on the capacitor is dissipated via NMOS to ground. Thus, in the complete cycle of charging & discharging, total energy dissipated is $E = C_{LOAD} .V_{DD}^2$ which contributes to the switching power dissipation.

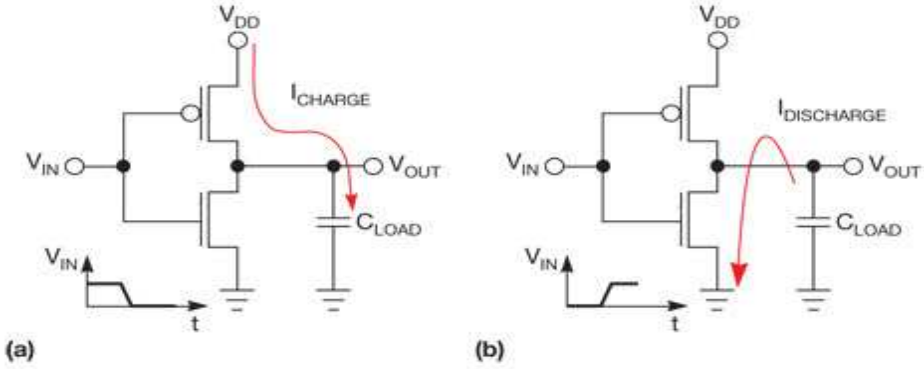

Fig.1. Charging and discharging of a CMOS inverter

Switching power dissipation can be expressed as:

$$P_D = \alpha C_L V_{DD}^2 f$$

where α is the switching activity,
f is the operation frequency,
C_L is the load capacitance,
V_{DD} is the supply voltage.

Thus the switching power dissipation can be reduced by reducing either the clock frequency f, or the load capacitance C_L, or the rail voltage V_{DD}, or the switching activity parameter α .Switching activity can be defined as the average number of transitions per clock cycle. The reduction of power supply voltage is one of the most aggressive techniques because the power savings are significant due to the quadratic dependence of V_{DD}. Although such reduction is very effective, a designer has to deal with several important issues to avoid decrease of the system performance. Specifically, the reduction of the power supply voltage leads to an increase in the propagation delay. Switching power can be minimized by reducing average number of transitions per clock cycle i.e. switching activity. The reduction of switching activity requires a detailed analysis of signal transition probabilities and implementation of various circuit-level design techniques.

2.2.2 Short circuit Power Dissipation

Short circuit power occurs when both PMOS & NMOS are conducting simultaneously and thus creating a direct path from V_{DD} to GND. In sequential circuits, all the operations are executed either on positive or on negative edge of clock pulses but at the same time, clock transitions cause major power dissipation in CMOS devices due

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to short circuit current dissipation which contributes almost 15-45% of the total power dissipation in a system. This can be explained with the help of a CMOS inverter as shown in Fig. 2.and its simulation in Fig.3.

In a CMOS inverter, when logic 1 is applied at the input of NMOS and PMOS, NMOS will conduct and PMOS is off, providing logic 0 at the output. When logic 0 is applied at the input, then PMOS will conduct and NMOS is in off state so logic 1 appears at the output. Every clock pulse has a certain rise time & fall time which is very small as compared to the period of a clock (e.g. if clock pulse has a period of 1 us then clock edge rise and fall times are 0.01µs) but it cannot be neglected when measuring the power dissipation in the system. At some point of clock transition, both NMOS and PMOS are conducting simultaneously, creating a short circuit path between V_{DD} and ground. Therefore, comparatively large amount of current flows for a very short period of time through that path causing short circuit power dissipation which occurs at every signal transition.

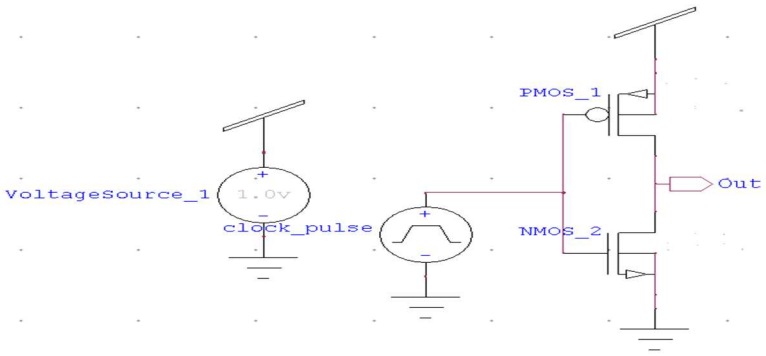

Fig. 2. Schematic of a CMOS Inverter

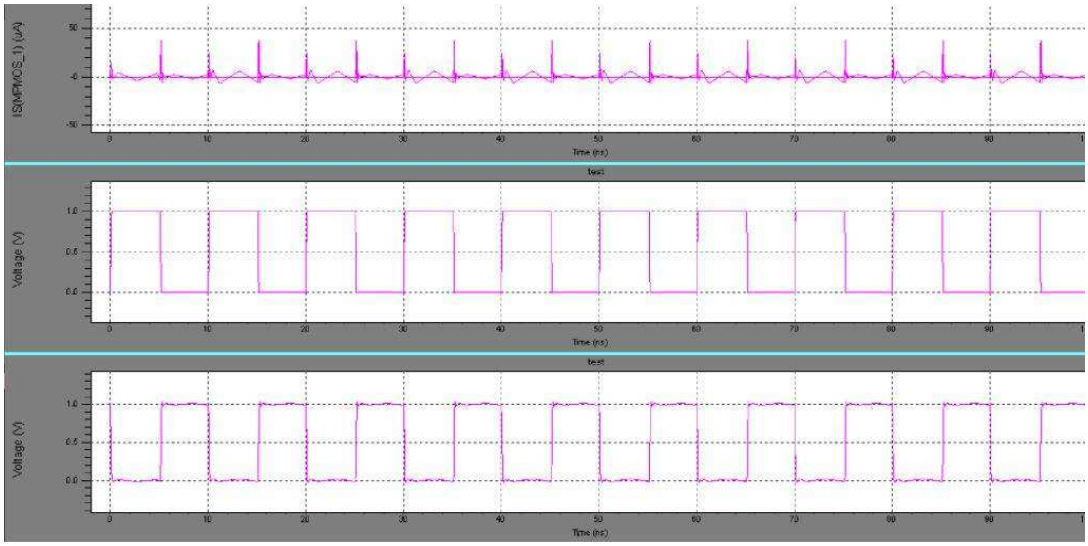

Fig. 3 Short circuit current at clock transitions

Normally in CMOS micro devices, currents are rated at nano-Ampere (nA) but from fig.3, it can be observed that the current flows in micro-Ampere (µA) range at each clock transition for a very short time, causing major power dissipation in the system. As this current spike appears at clock transition switching mode, this is known as switching mode short circuit current and causes short circuit power dissipation.

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3. RESULTS AND DISCUSSION

The simulations of the proposed design along with conventional & clock gated design of a 4-bit Johnson counter has been performed on TANNER v14.1 EDA tool in 90 nm CMOS technology. Tanner EDA is a suite of tools which allow you to enter schematics, perform SPICE simulations, do physical design (i.e. Chip layout), and perform design rule checks (DRC) and layout versus schematic (LVS) checks of analog, mixed-signal, RF and MEMS ICs .There are 3 tools that are used for this process:

1. S-Edit- a schematic capture tool.
2. T-SPICE- the SPICE simulation engine integrated with S-edit.
3. L-Edit- the physical design tool.

Fig 4 shows the operation of a 4-bit conventional Johnson counter where all the flip-flops are getting clock pulses at every state. Data are shifting at every state by the D flip-flop. It is observed that in most of the cases, this shifting is unnecessary. In each flip-flop, in a total of 8 pulses, only at 2 pulses data are changing. So, at every flip-flop, unnecessary data shifting are occurring in 6 pulses out of 8. In one cycle, a total of 32 clock pulses are required to operate a 4 bit Johnson Counter where only 8 clock transitions are effective to operate the design and remaining clock transitions can be eliminated as they cause unnecessary power dissipation.

The simulations for the clock gated Johnson counter is shown in fig.5 where it can be observed that each flip flop is getting clock pulses when it needs to toggle the value stored in it. In a total of 8 clock pulses (one cycle), each flip-flop is provided only 2 clock pulses at different state by the clock gating system only when the data needs to be toggled. Clock gating system is processing the stored value in each flip-flop at every state and allowing clock to certain flip flop only when it requires toggling the value in it. Thus it is ensured in the system that there will be no unnecessary clock operations which will eliminate all unnecessary power dissipations for inactive clock transitions. So, theoretically power dissipation due to clock transitions has been minimized by 75% in clock gated system. But practically the power dissipation minimization rate is not that dramatic as some additional combinational circuitry as clock gating system is used. But it has been observed that overall power dissipation of the clock gated system is much lower than that of conventional design.

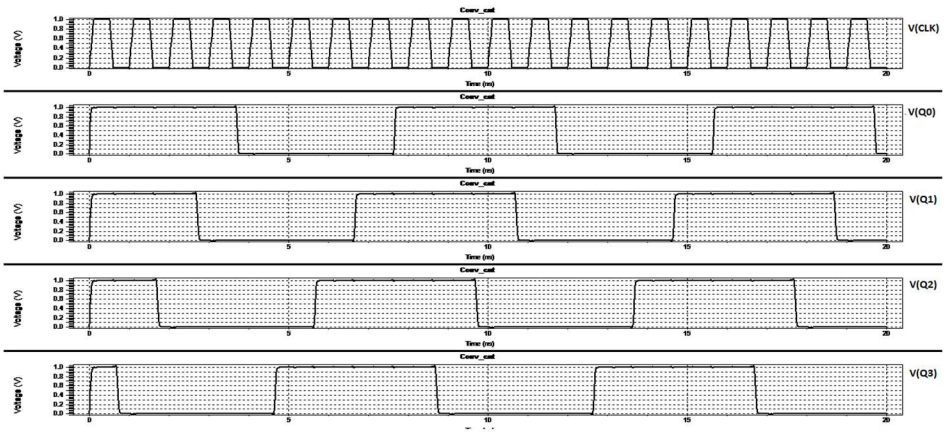

Fig.4 Simulation of a 4 –bit Conventional Johnson counter.

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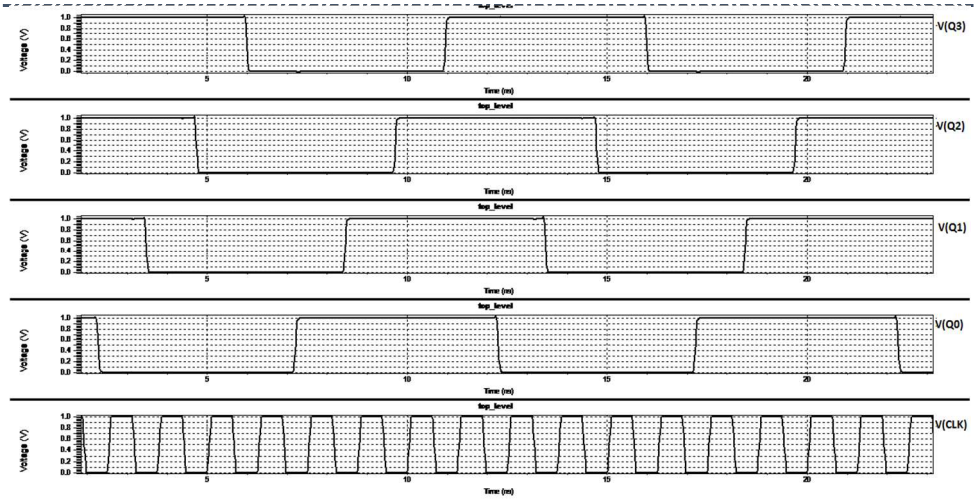

Fig.5 Simulation of a 4 –bit clock gated Johnson counter

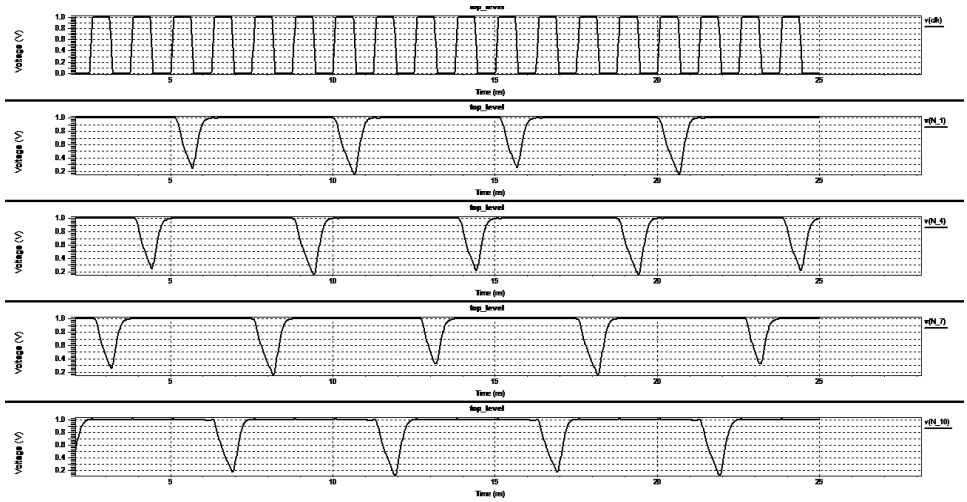

Fig.6 Output of Clock gated system

The simulations for the Modified Johnson counter design is shown in Fig.6.Clock gating system processes the stored value in each flip-flop at every state and allowing clock to certain flip flop only when it requires toggling the value in it. The clock pulse sequences generated from the clock gated unit are entered into pulse generation circuit of the pulse-triggered flip flop where the clock pulses are made very narrow in width around the falling edge of the clock which acts as clock input to the latch. Pulse –triggered flip flop used in the proposed design is of implicit type where the clock distribution circuit is a built in logic and there is no need for an external circuitry for the clock division and distribution.

4. CONCLUSION

This dissertation presents an improved pulse –triggered flip flop based low power 4-bit Johnson Counter design. The design has been simulated and results are compared with that of the conventional & clock gated counter design. It has been observed that the proposed design shows a power reduction of 66.73% as compared to the conventional Johnson counter & 44.76% as compared to clock gated counter design. The power dissipation of proposed design ranges from 36.68µW to 54.69µW for frequency ranging from 600MHz to 1GHz.

The power analysis for two flip flop designs shows that Modified pulse triggered flip flop can save power up to 39.67% as compared to Conventional Master Slave flip flop. The Pulse-triggered flip flop used in the proposed

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design contain 19 transistors whereas traditional Master Slave flip flop has a transistor count of 34. Also, average power dissipation of XOR & XNOR gates designed using GDI technique is much lower than CMOS based logic gates while maintaining lower complexity of the design. XOR & XNOR gates designed using GDI technique contains 8 & 6 transistors respectively whereas CMOS based logic gates require 13 & 11 transistors respectively. The proposed design of Johnson counter shows a significant reduction in power dissipation as compared to the conventional & clock gated design. The techniques used for implementing the proposed system can be extended to any sequential circuit design where power minimization is an important constraint.

As it is noticed that the proposed design of Johnson counter contributes to major reduction in power dissipation, future research to develop a more power efficient flip flop architecture & clock gating system for not only Johnson Counter but also other important sequential devices. In future, the delay produced by the clock gating circuitry should be minimized for integrating clock gating system .Also speed and delay consideration should be developed for.

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